DVB-S2 HIGH THROUGHPUT LDPC ENCODER

IP CORE

C-LDPC-HT-ENC-2479

OVERVIEW

The DVB-S2 standard is designed for broadcast services, interactive services, digital satellite news gathering, and professional services. DVB-S2 became the first standard to adopt low-density parity-check (LDPC) codes. DVB-S2 offers a powerful forward error correction (FEC) based on LDPC codes and allows quasi error-free operation at about 0.7 dB to 1 dB from the Shannon limit which yields better decoding performance.

The C-LDPC-HT-ENC-2479 is a high throughput low latency LDPC error correction encoder compliant with Digital Video Broadcasting Satellite Second Generation standard (DVB-S2 ETSI EN 302 307 V.1.4.1) specifications.

It supports both short and normal frames. C-LDPC-HT-ENC-2479 achieves high throughput at low clock frequencies. Input rate, throughput and latency are given in the table below for 175 MHz clock frequency.

Short Frame				
Identifier	**Effective Rate**	**Input Rate** (Gbps)	**Throughput** (Gbps)	**Latency** (μs)
1/4	1/5	0.525	2.62	4.07
1/3	1/3	0.837	2.51	4.31
2/5	2/5	0.975	2.44	4.49
1/2	4/9	1.13	2.54	4.21
3/5	3/5	1.35	2.25	5.00
2/3	2/3	1.61	2.41	4.49
3/4	11/15	1.81	2.47	4.31
4/5	7/9	1.94	2.49	4.26
5/6	37/45	1.99	2.43	4.42
8/9	8/9	2.14	2.41	4.43

Normal Frame				
Identifier	**Effective Rate**	**Input Rate** (Gbps)	**Throughput** (Gbps)	**Latency** (μs)
1/4	1/4	1.64	6.61	7.57
1/3	1/3	1.99	6.03	8.43
2/5	2/5	2.24	5.63	9.12
1/2	1/2	2.77	5.58	9.12
3/5	3/5	2.81	4.71	11.2
2/3	2/3	3.64	5.50	9.12
3/4	3/4	3.90	5.24	9.63
4/5	4/5	4.03	5.07	9.99
5/6	5/6	4.11	4.96	10.02
8/9	8/9	4.80	5.44	9.03
9/10	9/10	4.84	5.42	9.06

C-LDPC-HT-ENC-2479 IP Core is compatible with Xilinx Zynq UltraScale+ MPSoCs family.

DELIVERABLES

The deliverables are given below.

- VHDL source code or synthesized netlist
- HDL simulation models
- Matlab simulation model
- Documentation

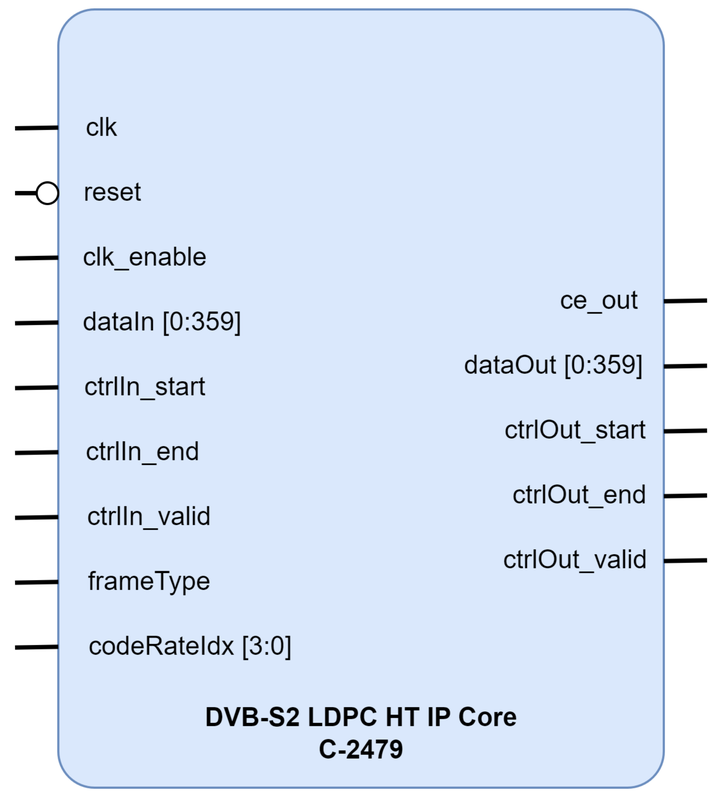
DEVICE UTILIZATION SUMMARY

The utilization report for Xilinx xczu7ev device is given in the table below.

DVB-S2 LDPC High Throughput Encoder Utilization		
Site Type	**Usage**	**Util % (xczu7ev)**
Registers	5772	1.75
LUTs	19912	8.64
BRAM	5	1.6
DSP	0	0

IOs

The C-LDPC-HT-ENC-2479 IP Core block diagram and input output ports are given below.



- **INPUT PORTS**
  - clk
    The synchronous clock is responsible for driving design block. Maximum clock frequency is 175 MHz. Data type is Boolean. All synchronous operations within the core occur to the rising edge of clk.
  - reset
    Reset signal sets the encoder to a known initial state. Data type is Boolean. The reset is active high.
  - clock _enable
    Data type is Boolean.
  - ctrlIn _start
    Start control signal for the input data, specified as a Boolean scalar.
  - ctrlIn _valid
    Valid control signal for the input data, specified as a Boolean scalar.
  - ctrlIn _end
    End control signal for the input data, specified as a Boolean scalar.
  - frameType
    Selects the frame type. 0 indicates the normal frame, 1 indicates the short frame. Data type is Boolean scalar.
  - codeRateIdx
    Selects LDPC code rates. 4 bit ufix4 data.
  - dataIn
    Input payload data, specified as a Boolean vector.
- **OUTPUT PORTS**
  - ce _out
    clock _enable output singal, specified as a Boolean scalar.
  - ctrlOut _start
    Start control signal for the encoded output data, specified as a Boolean scalar.
  - ctrlOut _valid
    Valid control signal for the encoded output data, specified as a Boolean scalar.
  - ctrlOut _end
    End control signal for the encoded output data, specified as a Boolean scalar.
  - dataOut
    Encoded output data, specified as a Boolean vector.

CONTACT INFORMATION

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